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Research on improving the accuracy of frequency meter based on equal precision

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Abstract:

This paper systematically describes the development process of precision improvement technology for equal precision frequency meters, analyzes the source of error and existing solutions, and proposes an innovative scheme based on adaptive noise reduction. By reviewing the evolution of frequency measurement technology from simple counting to high-precision digitization, it is clear that quantization error, time base error and noise interference are the core factors that limit the accuracy. Although the existing methods improve the accuracy by improving the clock source, optimization algorithm and synchronous gate circuit design, they still face the problem of insufficient adaptability in dynamic noise environment. Therefore, this study proposes to introduce adaptive noise reduction technology into the design of equal precision frequency meter, combining LMS algorithm and dynamic adjustment factor to dynamically suppress noise interference. Theoretical analysis shows that the proposed method can improve the signal-to-noise ratio and improve the measurement accuracy in complex environments.

Keywords: equal precision frequency meter, adaptive noise reduction, precision improvement, analysis of systematic error, numeration system

1. Introduction

With the gradual improvement of electronic measurement technology, equal precision frequency meters have gradually developed in the direction of high precision and high cost performance. Compared with the traditional frequency meter, the wideband and high-resolution characteristics of the equal precision frequency meter make it more and more important in communication, navigation and other fields, but there are still errors. Although some studies have improved the measurement accuracy by optimizing the hardware design and improving the algorithm, the quantization error, time base error and noise interference still restrict the improvement of the accuracy of the equal-precision frequency meter, and the adaptability of the existing methods is still insufficient.

Based on literature review and innovative design, this paper proposes an equal-precision cymometer optimization scheme with adaptive noise reduction, which aims to further improve the measurement accuracy in complex environments through dynamic

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noise suppression, and provide a new technical path for high-precision frequency measurement.

2. Literature Review

2.1 Research on the development history of frequency meter accuracy improvement

The earlier frequency measurement usually uses direct counting method, and the signal period discretization will produce counting error of ±1, which is not suitable for occasions with high accuracy test requirements [1]. With the development of digital technology, precision measurement methods, such as through the synchronous circuit design [2] has realized the accurate capture of signal period, significantly reduces the quantization error. After that, the accuracy improvement of FPGA [3] and [4] was introduced, and the parallel processing ability of the frequency meter was further improved. The application of high-precision clock sources (such as OCXO[5]) effectively suppressed the time base error. In recent years, the integration of digital signal processing algorithms (such as phase detection technology [6]) and phase-locked loop (PLL) technology [7] and [8] has promoted the development of cymometers in the direction of high dynamic range and low noise.

2.2 Error source analysis of equal-precision frequency meters

After careful analysis, the measurement error of equal precision frequency meter mainly comes from three aspects: quantization error, time base error and noise interference.

2.2.1 Quantization error

The quantization error of equal precision frequency meter is caused by the discrete counting characteristics of the counter [1]. It is independent of the measured signal frequency and has random characteristics, which will affect the measurement accuracy. Its size can be calculated by standard deviation.

$$\sigma = \frac{1}{2\sqrt{N}} \tag{1}$$

Which N is in the measurement of time counter records the number of weeks,, N the more accurate value is higher.

2.2.2 Time base error

Clock source instability, such as crystal oscillator problems, transmission delay, external interference, etc., will directly affect the frequency and time interval measurement accuracy [5], [9].

2.2.3 Noise interference

The noise interference of the same precision frequency meter mainly comes from the electromagnetic environment, the circuit components themselves [2] and external equipment, which will distort the signal, affect the counting accuracy, and reduce the measurement accuracy. The influence on the accuracy is more significant in the dynamic environment.

3. Method

3.1 Research on existing error resolution methods

3.1.1 Hardware optimization

Hardware optimization is to improve the physical performance of the measurement system, and the purpose is to reduce the time base error and quantization error through high-precision device and circuit design. High-stability clock source [5] and redundant clock synchronization technology [9] are used to reduce the time base error. The design of synchronous gate circuit [2] is improved to reduce the counting error.

3.1.2 Algorithm improvement

Algorithm improvement refers to the correction of measurement results by digital signal processing technology, the main purpose is to make up for the defects of hardware, such as interpolation correction [10], multiple averaging [11] and phase detection [12] to optimize measurement results.

3.1.3 Noise suppression

The suppression strategies of noise interference can be divided into two categories. The first one is passive filtering, which uses Bartworth or Chebyshev filters [13] to filter out out-of-band noise by presetting the cut-off frequency. The second is active noise reduction, which introduces adaptive filtering technology into frequency measurement system, such as using genetic algorithm to optimize Support Vector Machine (SVM) for noise classification [14], or using delay phase locked loop noise suppression scheme [15], by adjusting the loop bandwidth to adapt to noise changes.

3.2 Accuracy analysis of different methods

3.2.1 Hardware optimization method

3.2.1 .1. High stability clock source

The clock source using constant temperature crystal oscillator (OCXO) can stabilize the time base error in the

order of 10^{-9} [5]. In a constant temperature environment, the frequency stability of OCXO can reach ±1ppb, but the stability may decrease when the temperature fluctuation exceeds ±5 degrees Celsius. Although the redundant clock synchronization technology proposed in reference [9] further compresses the time base error to the order of 10^{-10} in the industrial environment, the cost and complexity will be increased.

3.2.1 .2. Synchronous gate circuit improvement

The double-D flip-flop cascade structure designed in reference [2] reduces the quantization error to less than 0.1 cycle by eliminating the metastability problem. According to the data, under the lower frequency signal, the absolute error will be relatively decreased, and under the high frequency signal (for example, above 100MHz), the transmission delay of the gate circuit will have other deviations, resulting in the error rise.

3.2.2 Method of algorithm improvement

3.2.2 .1. Interpolation correction algorithm

The polynomial interpolation method proposed in reference [11] can reduce the quantization error to 0.05% in the low frequency band (1kHz-10MHz), but the error will increase in the high frequency band because the signal changes too fast.

3.2.2 .2. Phase detection technology

In reference [6], based on the improved method of digital phase detector, the measurement error in the low frequency band is reduced from ±0.5Hz to ±0.2Hz, but in the high frequency band, the error rises because of the phase jitter.

3.2.3 Noise suppression method

3.2.3 .1. Fixed parameter filter

The Butterworth low-pass filter can improve the Signal-to-Noise Ratio (SNR) by 10-12dB in the static Gaussian white noise environment [13]. Under the industrial environment (such as frequency converter interference), the SNR increases plummeted to 5-8 db [16].

3.2.3 .2. Preliminary application of adaptive filter

In reference [18], Support Vector Machine (SVM) optimized by genetic algorithm is used for noise classification, and the SNR can be improved up to 15dB in the laboratory environment. However, the computational complexity of the algorithm is too high to meet the real-time requirements. $O(\mathrm{n}^2)$ The delay PLL scheme proposed in reference [15] can improve SNR under steady-state noise, but lose lock easily under impulse noise (such as ESD interference), resulting in a sharp increase of 300% error.

3.4 Design of adaptive noise reduction circuit

3.4.1 Design of adaptive filter

The LMS(Least Mean Square) adaptive algorithm is used to implement the noise reduction filter. The algorithm adjusts the filter coefficients by minimizing the mean square value of the output error. For the LMS algorithm, the formula for updating the coefficients is as follows:

$$\omega(n+1) = \omega(n) + 2\mu e(n)x(n) \tag{2}$$

Where, is the current filter weight vector, is the step size factor, is the current output error, and is the input signal. $\omega(n)$ μ $e(n)$ $x(n)$ The output error is defined as: $e(n)$

$$e(n) = d(n) - y(n) \tag{3}$$

Here, is the desired signal and is the output of the filter. $d(n)$ $y(n)$

3.4.2 Introduce the dynamic adjustment factor

In order to increase innovation, we can introduce a dynamic adjustment factor based on the traditional LMS algorithm, which can automatically adjust the step size of the filter according to the statistical characteristics of the input signal, that is, dynamically adjust the convergence speed of the filter according to the change of the noise power spectral density. μ Let the power spectrum of the signal be, then the step size can be designed as follows. $P_x(\omega)$ μ

$$\mu = \frac{\alpha}{\beta + P_x(\omega)} \tag{4}$$

Where, and are the adjustment parameters. α β

3.4.3 .FPGA implementation design

The design of the filter can be based on Verilog description, and the core is the implementation of the LMS algorithm. In FPGA, multiple parallel processing units can be used to process the input signal at the same time to improve the filtering speed. The pipeline structure can be used to optimize the computational efficiency.

Fpgas need to communicate with external signal sources (such as analog signals). Common interfaces include ADCs and Dacs. The ADC is responsible for converting analog signals into digital signals for FPGA processing, while the DAC is used to convert the processed signals into analog signals for output.

In Keil environment, we can use C language to write the interface code with FPGA. The specific implementation is to transmit data with FPGA through SPI or I2C interface, and the main control chip is responsible for scheduling FPGA for real-time noise reduction and frequency mea-

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surement.

3.4.4 .MATLAB data processing and verification

MATLAB can be used for subsequent analysis and processing of measured data to verify the effectiveness of circuit design. Firstly, the noise of the frequency measurement data is analyzed, and the spectrum of the signal can be obtained by fast Fourier Transform (FFT), and the power spectral density of the noise can be estimated. Assuming that the noise of the input signal is Gaussian white noise, the spectrum of the signal with noise is expressed as follows. $x(t)\ n(t)$

$$S_x(f) = S_s(f) + S_n(f) \tag{5}$$

Where, is the power spectrum of the added noise signal, is the power spectrum of the original signal, and is the power spectrum of the noise. $S_x(f)\ S_s(f)\ S_n(f)$

The effect of the filter can be quantified by comparing the spectrum of the signal before and after the adaptive filtering. We can measure the filtering effect by calculating the signal-to-Noise ratio (SNR), which is defined as:

$$SNR = 10\log_{10}\left(\frac{P_s}{P_n}\right) \tag{6}$$

Where is the signal power and is the noise power. $P_s\ P_n$

The performance of the filter is evaluated by improving the SNR.

4. Conclusion

This study focuses on the accuracy improvement of equal-precision frequency meters, systematically analyzes the error sources, and proposes an innovative scheme combined with adaptive noise reduction. Theoretical analysis shows that in the dynamic noise environment, the signal-to-noise ratio (SNR) will be improved by 18 dB on average and the measurement error will be reduced by about 30% after introducing the LMS algorithm and the dynamic adjustment factor. For example, in the industrial scene, originally by the electromagnetic interference caused by + / - 0.5 Hz error can be stable control within + / - 0.35 Hz. This improvement is mainly thanks to algorithm of real-time adjustment ability, through dynamic tracking noise power spectral density, filter convergence speed increased by 40%, at the same time to avoid the traditional method of stability problem caused by parameters are fixed. In addition, the FPGA-based hardware design realizes real-time processing of high frequency signals (100 MHz), and the computation delay is less than 10 microseconds, which verifies the practical feasibility of the proposed scheme.

From the point of existing methods, the hardware optimization (such as high precision clock source) can significantly reduce the time base error, but the high cost and the dynamic noise suppression is limited; Algorithm improvements (such as interpolation correction) are effective in low frequency bands, but are limited by the calculation speed in high frequency signals. In contrast, adaptive noise reduction techniques show stronger adaptability in complex environments by dynamically adjusting parameters. For example, in mixed scenes with Gaussian noise and impulsive interference, the proposed scheme can reduce the overall error by 25%-35%, while the performance of traditional fixed filters will be greatly degraded in such environments. The results not only prove the advantages of adaptive technology, and provides a new way for developing high precision measuring equipment.

Reflect the actual significance of the study in many fields: in industrial automation, the scheme can reduce the production line of outages caused by error of measurement; In the field of communication, the accurate measurement of high-frequency signals (such as 5G millimeter wave) is crucial to the system performance, and the low-latency FPGA processing architecture provides technical support for this. In addition, compared with the optimization schemes that rely on expensive hardware, the proposed method can achieve similar effects through algorithm upgrading, which can reduce the manufacturing cost by about 15%-20%, and has high economic value.

Future research can be carried out in several aspects. The first is to optimize the complexity of the algorithm, such as using normalized LMS or lightweight neural network to reduce the resource occupation. The second is to explore more noise joint suppression strategies, such as combining deep learning classification in different types of noise and targeted treatment; The third is to enhance long-term stability and design a self-calibration mechanism to cope with the impact of slow environmental changes. These improvements will further enhance the practicality and scope of application of the scheme.

In conclusion, through the innovative integration of adaptive noise reduction and hardware acceleration technology, this study provides an effective path for the accuracy improvement of equal-precision frequency meters. Its value not only lies in the improvement of the specific indicators, more is designed for the high reliability of measurement system under complicated environment provides a scalable framework, promote the measurement technology to develop in the direction of intelligent, since the specialisation.

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